IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1(Original). A test system comprising:

a burn-in configuration register;

combinational logic operational in response to IC Die identification (ID) scan data and burn-in configuration register data to generate Die ID scan out signals;

means for generating memory built-in self-test (BIST) signals;

means for generating scan chain signals; and

exclusive-OR logic operational in response to the Die ID scan out signals, memory BIST signals, and scan chain signals to generate monitored output signals.

2(Original). The test system according to claim 1, wherein the burn-in configuration register comprises:

a Die ID Scout Enable register;

a plurality of Scout Chain Enable registers, and

a Memory BIST status enable register.

3(Original). The test system according to claim 1, wherein the combinational logic comprises AND logic.

4(Original). A test system comprising:

means for configuring the test system;

means for generating Die identification (ID) scan out signals;

means for generating memory built-in self-test (BIST) signals;

means for generating scan chain signals; and

exclusive-OR logic operational in response to the Die ID scan out signals, memory BIST signals, and scan chain signals to generate monitored output signals.

5(Original). The test system comprising according to claim 4, wherein the means for configuring the test system comprises a burn-in configuration register.

6(Original). The test system comprising according to claim 5, wherein the means for generating Die ID scan out signals comprises combinational logic operational in response to IC Die identification (ID) scan out data and burn-in configuration register data to generate the Die ID scan out signals.

7(Original). The test system according to claim 6, wherein the combinational logic comprises AND logic.

8(Original). The test system according to claim 5, wherein the burn-in configuration register comprises:

a Die ID Scout Enable register; and

a plurality of Scout Chain Enable registers.

9(Original). The test system according to claim 8, wherein the burn-in configuration register further comprises a memory built-in self-test (MBIST) Fail Enable register.

10 – 14. Canceled.

15(New). A method of testing integrated circuit failures on a test system comprising:

configuring test system;

generating Die identification (ID) scan out signals;

generating memory built-in self-test (BIST) signals;

generating scan chain signals; and

generating monitored output signals, wherein the monitored output signals are generated using exclusive-OR logic operation in response to the Die ID scan out signals, memory BIST signals, and scan chain signals.

16(New). A method according to claim 15, wherein configuring the test system comprises configuring a burn-in configuration register.

17(New). A method according to claim 16, wherein the Die ID scan out signals are generated by a combinational logic operational in response to IC Die identification (ID) scan out data and burn-in configuration register data.

18(New). A method according to claim 17, wherein the combinational logic comprises AND logic.

19(New). A method according to claim 16, wherein the burn-in configuration register comprises:

a Die ID Scout Enable register; and

a plurality of Scout Chain Enable registers.

20(New). A method according to claim 19, wherein the burn-in configuration register further comprises a memory built-in self-test (MBIST) Fail Enable register.